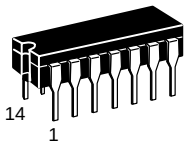
Clock Driver Quad D-Type Flip-Flop
With Matched Propagation Delays

MC74F803

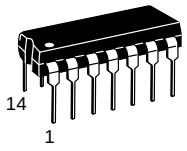
CLOCK DRIVER QUAD D-TYPE FLIP-FLOP WITH MATCHED PROPAGATION DELAYS

The MC74F803 is a high-speed, low-power, quad D-type flip-flop featuring separate D-type inputs, and inverting outputs with closely matched propagation delays. With a buffered clock (CP) input that is common to all flip-flops, the F803 is useful in high-frequency systems as a clock driver, providing multiple outputs that are synchronous. Because of the matched propagation delays, the duty cycles of the output waveforms in a clock driver application are symmetrical within 1.0 to 1.5 nanoseconds.

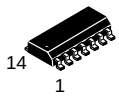
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Matched Outputs for Synchronous Clock Driver Applications
- Outputs Guaranteed for Simultaneous Switching



J SUFFIX
CERAMIC
CASE 632-08

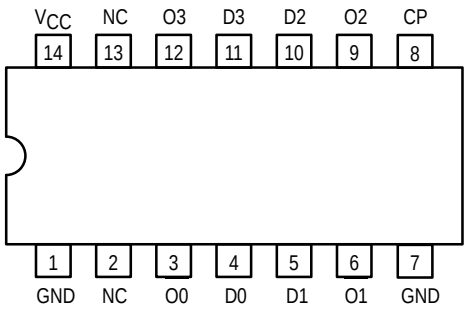


N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-03

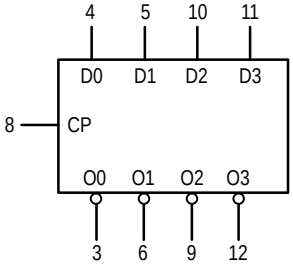
Pinout: 14-Lead Plastic (Top View)



GUARANTEED OPERATION RANGES

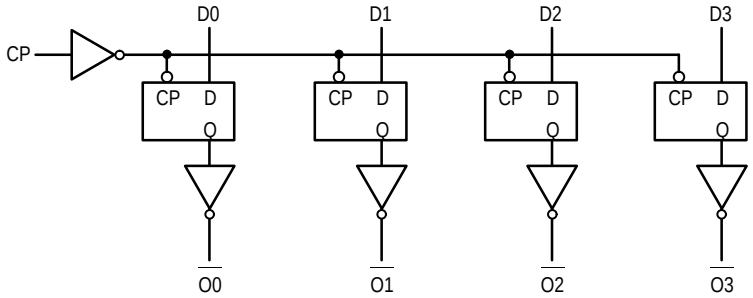
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High	—	—	–20	mA
I_{OL}	Output Current — Low	—	—	24	mA

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PINS 1 AND 7
NC = PINS 2 AND 13

LOGIC DIAGRAM



MOTOROLA

FUNCTIONAL DESCRIPTION

The F803 consists of four positive edge-triggered flip-flops with individual D-type inputs and inverting outputs. The buffered clock is common to all flip-flops and the following specifications allow for outputs switching simultaneously. The four flip-flops store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. The maximum frequency of the clock input is 70 megahertz, and the LOW-to-HIGH and HIGH-to-LOW propagation delays of the O_1 output vary by, at most, 1 nanosecond. Therefore, the device is ideal for use as a divide-by-two driver for high-frequency clock signals that require symmetrical duty cycles. The difference between the LOW-to-HIGH and HIGH-to-LOW propagation delays for the O_0, O_2, and O_3 outputs vary by at most 1.5 nanoseconds. These outputs are very useful as clock drivers for circuits with less stringent requirements. In addition, the output-to-output skew is a maximum of 1.5 nanoseconds. Finally, the I_{OH} specification at 2.5 volts is guaranteed to be at least – 20 milliamps. If their inputs are identical, multiple outputs can be tied together and the I_{OH} is commensurately increased.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions*	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0	—	—	V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	—	—	0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage	—	—	– 1.2	V	I_{IN} = –18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	2.5	—	—	V	I_{OH} = –20 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	—	0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
		—	—	20	µA	V_{IN} = 2.7 V	V_{CC} = MAX
I_{IH}	Input HIGH Current	—	—	100		V_{IN} = 7.0 V	V_{CC} = MAX
I_{IL}	Input LOW Current	—	—	–0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)	–60	—	–150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current	—	—	70	mA	V_{CC} = MAX	

* Normal test conditions for this device are all four outputs switching simultaneously. Two outputs of the 74F803 can be tied together and the I_{OH} doubles.

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%, see Note 1)

Symbol	Parameter	C_L = 50 pF		C_L = 100 pF		Unit
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	70	—	50	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{On}$	3.0	7.5	3.0	10	ns
t_{Pv}	Propagation Delay CP to $\overline{On}$ Variation (see Note 3)	—	3.0	—	4.0	ns
t_{ps} $\overline{O_1}$	Propagation Delay Skew $\lvert t_{PLH}$ Actual – t_{PHL} Actual$\rvert$ for O_1 Only	—	1.0	—	2.0	ns
t_{ps} $\overline{O_0}$, O_2, O_3	Propagation Delay Skew $\lvert t_{PLH}$ Actual – t_{PHL} Actual$\rvert$ for O_0, O_2, O_3	—	1.5	—	2.0	ns
t_{os}	Output to Output Skew (see Note 2) $\lvert t_p$ $\overline{On}$ – t_p $\overline{Om}\rvert$	—	1.5	—	2.5	ns
t_{rise}, t_{fall} $\overline{O_1}$	Rise/Fall Time for $\overline{O_1}$ (0.8 to 2.0 V)	—	3.0	—	4.0	ns
t_{rise}, t_{fall} $\overline{O_0}$, $\overline{O_2}$, $\overline{O_3}$	Rise/Fall Time for $\overline{O_0}$, $\overline{O_2}$, $\overline{O_3}$ (0.8 to 2.0 V)	—	3.5	—	4.5	ns

1. The test conditions used are all four outputs switching simultaneously. The AC characteristics described above (except for O_1) are also guaranteed when two outputs are tied together.
2. Where t_p On and t_p Om are the actual propagation delays (any combination of high or low) for two separate outputs from a given high transition of CP.
3. For a given set of conditions (i.e., capacitive load, temperature, V_{CC}, and number of outputs switching simultaneously) the variation from device to device is guaranteed to be less than or equal to the maximum.

AC OPERATING REQUIREMENTS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%)

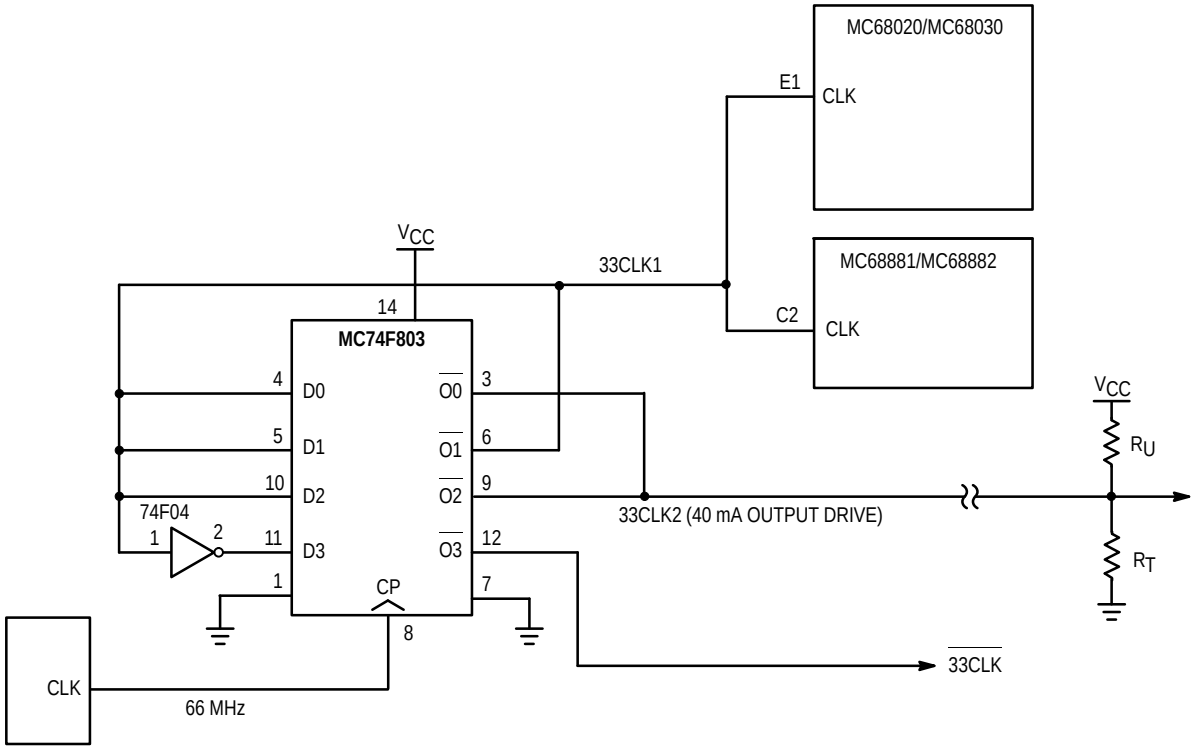
Symbol	Parameter	C_L = 50 pF		C_L = 100 pF		Unit
		Min	Max	Min	Max	
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW D_n to CP	3.0 3.0	— —	4.0 4.0	— —	ns
t_f	$t_p + t_s$ (see Note)	—	9.0	—	12	ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW D_n to CP	2.0 2.0	— —	2.0 2.0	— —	ns
$t_{w(H)}$ $t_{w(L)}$	CP Pulse Width HIGH or LOW	7.0 6.0	— —	8.0 8.0	— —	ns

The combination of the setup time (t_s) requirement and maximum propagation delay (t_p) are guaranteed to be within this limit for all conditions.

APPLICATION NOTE

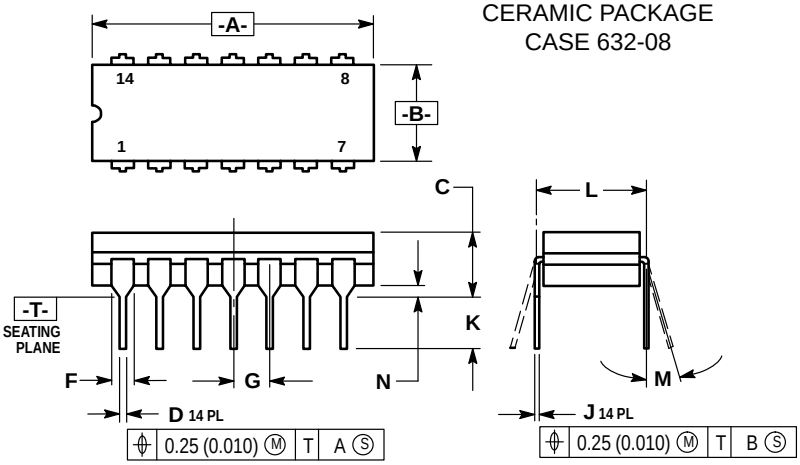
The closely matched outputs of the MC74F803 provide an ideal interface for the clock input of Motorola's high-frequency microprocessors.

74F803 INTERFACE AS CLOCK TO MC68020 SYSTEM



OUTLINE DIMENSIONS

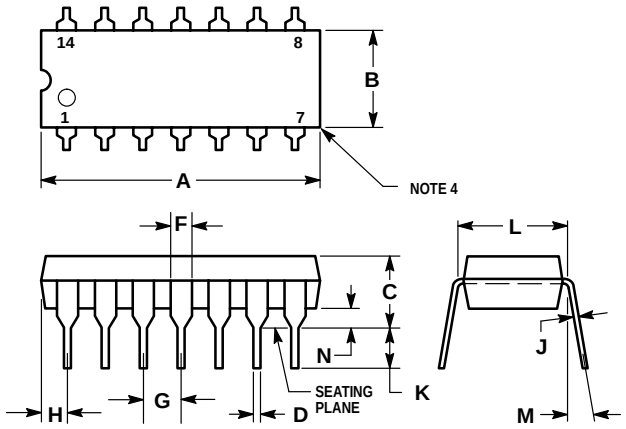
J SUFFIX
CERAMIC PACKAGE
CASE 632-08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

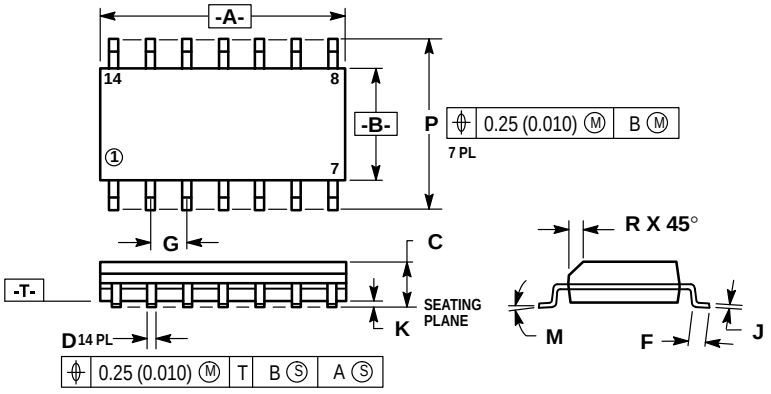
N SUFFIX
PLASTIC PACKAGE
CASE 646-06



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. 646-05 OBSOLETE, NEW STANDARD 646-06.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

D SUFFIX
SOIC PACKAGE
CASE 751A-02



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Literature Distribution Centers:
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