```
------------------------------------------------------------------------
Computing MAX delays for data through the CHIP RAM bridge path of BRIDGET:
------------------------------------------------------------------------


CPU read from CHIP RAM.  This path is thru the bridge if
the CPU is only 16 bits:

      RAS timing

             280    C1 cycle time
           - 35  data is latched 35 ns before C1 rises
           - 70  C1 high to C3 high
           - 18  Tcqrl (max) (C3 high to RAS low)
           - 80  RAS access time (max)
           - 10  'slop'
           ----
             67

      CAS timing ( Taa > Tcac + (max CAS delay thru PAL) )

             280  C1 cycle time
           - 35  data is latched 35 ns before C1 rises
           -140  C1 high to C1 low
           -  6  Tckcl (max) (C1 low to CAS low)
           - 40  Taa (max) (CAS adr access time)
           - 10  'slop'
           ----
             49

CPU write to CHIP RAM:

      Incredibly obviously OK ...

CHIP write to CHIP RAM on odd bank (thru bridge) (no double CAS):

             140  C1 high to CAS low (min)
           -125  Tchedo (max) (C1 high to early read data valid)
                       [** ALICE has value of 130 **]
           +  5  CAS delay thru PAL (min)
           - 10  'slop'
           ----
             10  (un oh...)
           + 35  delayed CAS to the rescue (writes only)
           ----
             45

CHIP read from CHIP RAM on odd bank (thru bridge) (no double CAS):

      RAS timing

             280  C1 cycle time
           - 70  C1 high to C3 high
           - 18  Tcqrl (max)
           - 80  RAS access time (max)
           - 50  Tdins (ALICE/PAULA, read at C1 rising)
           - 10  slop
           ----
             52
```

CAS timing

```
 280  C1 cycle time
-140  C1 high to C1 low
-  6  Tckcl (max)
- 40  Taa, CAS adr access time (max)
- 50  Tdins (ALICE/PAULA, read at C1 rising)
- 10  'slop'
----
  34
```

CHIP read from CHIP RAM (double CAS, done for LISA only):
(bridge is not invloved)

RAS timing

```
 140  RAS low to 1st CAS high (min)
- 80  RAS access time (max)
- 20  Tdins (LISA)
- 10  'slop'
----
  30
```

CAS timing

```
  70  CAS low 'til read (min)
- 40  Taa, CAS adr access time (max)
- 20  Tdins (LISA)
- 10  'slop'
----
   0
```

CHIP read from CHIP RAM on odd bank (double CAS, done for LISA only):

This NEVER needs to be done, because if an odd bank exists, then CHIP RAM must be 32 bits wide. Therefore, double CAS fetches should be done ONLY as 32 bits (hec, it barely makes it WITHOUT the bridge!).