REAL-TIME CLOCK WITH INTERNAL RAM

RP/RF5C01A

NO. EK-086-9804

OUTLINE

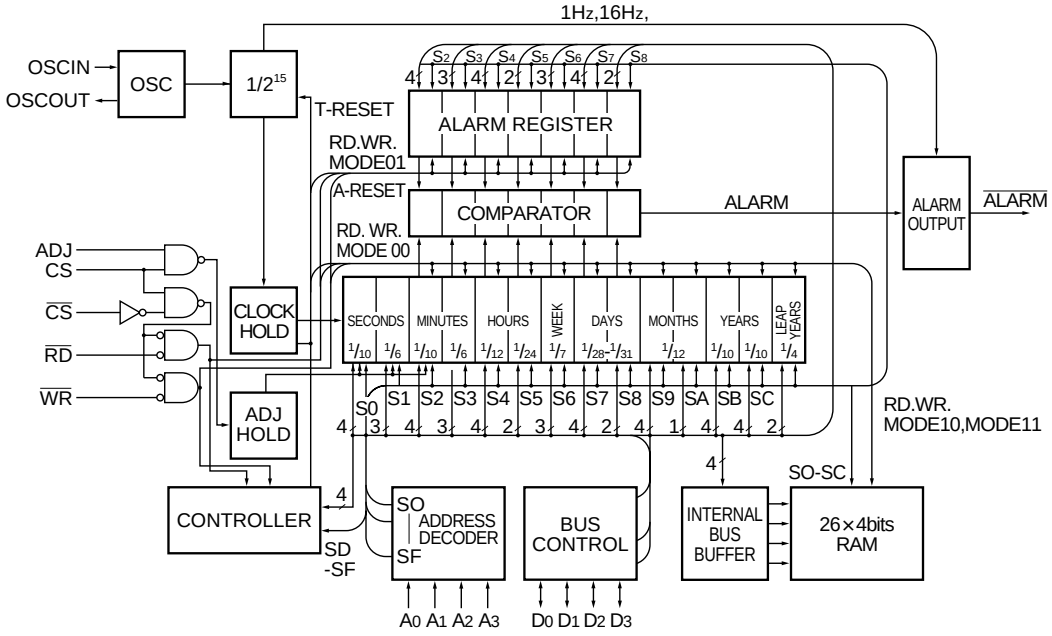
The RP/RF5C01A are real-time clocks for microcomputers that can be connected directly to buses of microcomputers with such CPUs as the 8085A or Z80 and allow setting or reading of the clock with the same procedures as for the Read/Write operation for memory.

These products have various features such as clock and calendar counters, alarm functions, and 26 × 4bits RAM which can be backed up by batteries. They can then be used as non-volatile RAM.

FEATURES

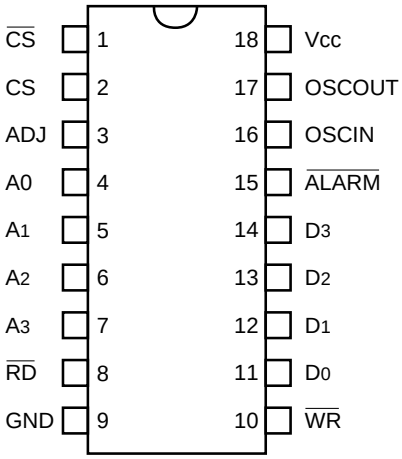
- Connected directly to CPU • 4bit bidirectional data bus : D0 - D3 • 4bit address input : A0 - A3
- Built-in clock counter (hour, minute, second) and calendar counter (leap year, year, month, day, day-of-the-week)
- Supports both 12-hour AM/PM clock and 24-hour clock
- All clock data expressed in BCD codes • ±30 second adjustment function
- Backed up by batteries (minimum:2.2V) • Built-in 26 × 4bits RAM
- Outputs alarm signals or timing pulse of 16Hz or 1Hz.
- Packages : 18pin DIP (RP5C01A) ; 18pin SOP(RF5C01A)

BLOCK DIAGRAM

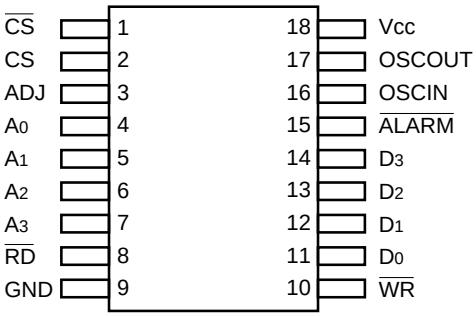


PIN CONFIGURATIONS

• **RP5C01A**



• **RF5C01A**



PIN DESCRIPTION

Pin No.	Symbol	Function
1,2	$\overline{CS}$,CS	The $\overline{CS}$ and CS are used to interface with external devices. Enabled when CS ="H" and $\overline{CS}$="L". The CS is connected to the power down detector in the system power supply while the $\overline{CS}$ is connected to the microcomputer.
3	ADJ	The ADJ can easily correct seconds without using the CPU. When this pin is set to "H" the second digits ranging from 00 to 29 are set to 0, the second digits ranging from 30 to 59 are set to 0 and minute digits are incremented by 1.
4,5,6,7	A_0 to A_3	Input pin for the address signal. These pins are connected to the CPU address bus.
8	$\overline{RD}$	Input pin for I/O control. The $\overline{RD}$ is set to "L" when data is transferred from the RP/RF5C01A to the CPU.
9	GND	Ground pin for the power supply of 0V.
10	$\overline{WR}$	Input pin for I/O control. The $\overline{WR}$ is set to "L" when data is transferred from the CPU to the RP/RF5C01A.
11,12,13,14	D_0 to D_3	Bidirectional data bus. Connected to the data bus of the CPU.
15	$\overline{ALARM}$	The $\overline{ALARM}$ pin outputs alarm signals and 16Hz and 1Hz clock pulses. This pin is an open drain output.
16,17	OSCIN,OSCOUT	The OSCIN and OSCOUT are connected to the crystal oscillator of 32.768kHz
18	V_{CC}	Input pin for the power supply of +5V.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Conditions	Ratings	Unit
V_{CC}	Supply Voltage	Referenced at GND pin	–0.3 to 7.0	V
V_I	Input Voltage		–0.3 to V_{CC}+0.3	V
V_O	Output Voltage		–0.3 to V_{CC}+0.3	V
Pd	Maximum Power Dissipation	Ta=25˚C	700	mW
Topr	Operating Temperature		0 to 70	˚C
Tstg	Storage Temperature		–40 to 125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, Ta=0 to 70˚C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{DH}	Data Preservation Voltage		2.2		5.25	V
f_{XT}	Crystal Oscillation Frequency			32.768		kHz

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=0 to 70˚C, Vcc=5V±10%)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	“H” Input Voltage (excluding OSCIN)		2.0		Vcc	V
	“H” Input Voltage (OSCIN)		4.0		Vcc	V
V_{IL}	“L” Input Voltage (excluding OSCIN)		–0.3		0.8	V
	“L” Input Voltage (OSCIN)		–0.3		0.5	V
V_{OH}	“H” Output Voltage	I_{OH}=–400µA	2.4			V
V_{OL}	“L” Output Voltage	I_{OL}=2mA			0.4	V
I_I	Input Voltage	V_I=0 to 5.25V			±10	µA
I_{OZ}	Output Off-state Leakage Current				±10	µA
I_{CC1}	Supply Current for backup	f_{XT}=32.768kHz, Vcc=2.2V			15	µA
I_{CC2}	Operating Supply Current	f_{XT}=32.768kHz, Vcc=5.0V*2			250	µA

*1) Plus (without sign) direction of current is assumed to be the direction flowing into IC.
*2) When connected to CPU (Read/Write cycle 10µs)

AC ELECTRICAL CHARACTERISTICS (Vcc=5V±5%)

(Ta=0 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
t_{AC}	Address–$\overline{RD}$/$\overline{WR}$ Delay Time		170			ns
t_{CC}	$\overline{RD}$/$\overline{WR}$ Pulse Width		400		10000	ns
t_{CA}	Address Effective Time after rising of $\overline{RD}$/$\overline{WR}$		10			ns
t_{RD}	Data Delay Time after falling of $\overline{RD}$				340	ns
t_{RDH}	Data Hold Time after rising of $\overline{RD}$		0			ns
t_{WDL}	Data Delay Time after falling of $\overline{WR}$				40	ns
t_{WD}	Data Hold Time after rising of $\overline{WR}$		20			ns

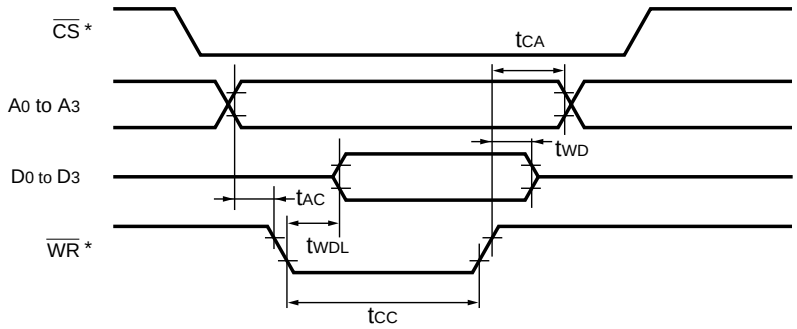
AC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%)

(Ta=0 to 70°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
t_{AC}	Address–$\overline{RD}$/$\overline{WR}$ Delay Time		170			ns
t_{CC}	$\overline{RD}$/$\overline{WR}$ Pulse Width		450		10000	ns
t_{CA}	Address Effective Time after rising of $\overline{RD}$/$\overline{WR}$		10			ns
t_{RD}	Data Delay Time after falling of $\overline{RD}$				400	ns
t_{RDH}	Data Hold Time after rising of $\overline{RD}$		0			ns
t_{WDL}	Data Delay Time after falling of $\overline{WR}$				40	ns
t_{WD}	Data Hold Time after rising of $\overline{WR}$		20			ns

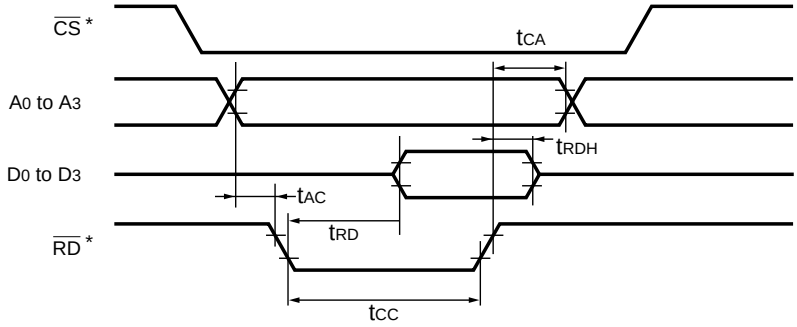
TIMING CHART

• Write Cycle (CS="H")



*) The RP/RF5C01A accept $\overline{WR}$ signals only when $\overline{CS}$="L" and CS="H". Although $\overline{CS}$ timing is not specified for the RP/RF5C01A, substitute $\overline{WR}$ signals shown above with $\overline{CS}$ · $\overline{WR}$ signals to be applicable to the RP/RF5C01A configuration.

• **Read Cycle (CS="H")**



*) The RP/RF5C01A accept $\overline{RD}$ signals only when $\overline{CS}$="L" and CS="H" as in the case of $\overline{WR}$ signals. Thus, substitute $\overline{RD}$ signals shown above, as in the case of $\overline{WR}$ signals, with $\overline{CS} \cdot \overline{RD}$ signals to be applicable to the RP/RF5C01A configuration.

ADDRESS MAPPING

MODE	MODE 00					MODE 01					10	11
A3 to A0	Description	D3	D2	D1	D0	Description	D3	D2	D1	D0	Description	Description
0	1-second counter						×	×	×	×	RAM 4bits×13 BLOCK 10	RAM 4bits×13 BLOCK 11
1	10-second counter	×					×	×	×	×		
2	1-minute counter					1-minute alarm register						
3	10-minute counter	×				10-minute alarm register	×					
4	1-hour counter					1-hour alarm register						
5	10-hour counter	×	×			10-hour alarm register	×	×				
6	Day-of-the-week counter	×				Day-of-the-week alarm register	×					
7	1-day counter					1-day alarm register						
8	10-day counter	×	×			10-day alarm register	×	×				
9	1-month counter						×	×	×	×		
A	10-month counter	×	×	×		$\overline{12}$/24 select register	×	×	×			
B	1-year counter					Leap year counter	×	×				
C	10-year counter						×	×	×	×		
D	MODE register	Timer EN	Alarm EN	MODE register M1	MODE register M0		Timer EN	Alarm EN	MODE register M1	MODE register M0	ditto	ditto
E	TEST register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0	ditto	ditto
F	RESET controller, etc.	$\overline{1Hz}$ ON	$\overline{16Hz}$ ON	Timer RESET	Timer RESET		$\overline{1Hz}$ ON	$\overline{16Hz}$ ON	Timer RESET	Alarm RESET		

*) "x" means "Don't care" for Write; always "0" for Read.

- **MODE register (Address Dh)**

D_3	D_2	D_1	D_0	
Timer EN	Alarm EN	M1	M0	
		↓	↓	
		0	0	MODE00 : Setting and read out of time
		0	1	MODE01 : Setting and read out of alarm, $\overline{12\text{-hour}}$/24-hour and leap year
		1	0	Read and Write of RAM of BLOCK10
		1	1	Read and Write of RAM of BLOCK11

→ 1 : Alarm output enabled
0 : Alarm output disabled
(Note that 16Hz or 1Hz signals are not affected.)

→ 1 : Counting time starts; 0 : the 1-second counter and higher-order than the 1-second counter stop

*) When the Timer EN is set to 0, the 1-second counter and higher-order counters than the 1-second counter stop . If any carrying occurs in the lower-order counters than the 1 second counter while the Timer EN is 0, carrying will be held and avoided when the Timer EN changes from 0 to 1. Thus, no apparent delay is produced when the duration of the Timer EN = 0 is less than one second.

- **$\overline{12}$/24 select register (MODE01, Address Ah)**

D_0=1 sets to 24-hour system ; D_0=0 sets to 12-hour system.
Set the 10-hour counter as D_1=1 for p.m., D_1=0 for a.m.

- **Leap year counter (MODE01, Address Bh)**

(D_1, D_0)=(0, 0) sets the counter for leap years. The counter value changes in order of (0, 0) (0, 1) (1, 0) (1, 1) (0, 0) repeatedly in the same timing as the year counter.

- **RESET controller/16Hz · 1Hz clock register. (Address Fh)**

D_0=1 : Resets all alarm registers.
D_1=1 : Resets divider stages for seconds or smaller units.
D_2=0 : 16Hz clock pulse ON.
D_3=0 : 1Hz clock pulse ON.

*) Addresses 0h to Dh are applicable both for Read and Write.
*) Addresses Eh to Fh are applicable only for Write.

OSCILLATOR CIRCUIT

- **When the oscillator circuit is to be configured using crystal oscillators:**

The oscillator circuit is configured as shown in Figure 1.

External components include: a resistor, a capacitor and a trimmer capacitor for fine tuning of the frequency. Adjust the trimmer capacitor (16Hz or 1Hz signal output from the $\overline{\text{ALARM}}$ pin is used) to correct oscillation frequency.

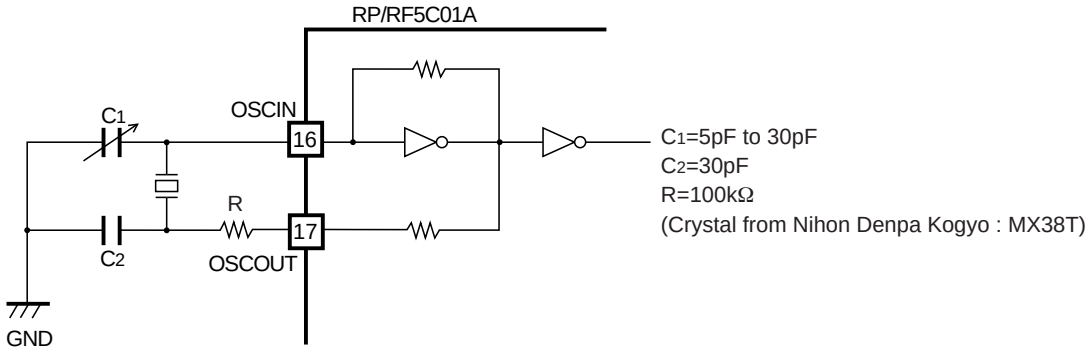
Correction with 16Hz signal:

Set addresses (A_3, A_2, A_1, A_0)=(1, 1, 1, 1).
Set Data (D_3, D_2, D_1, D_0)=(1, 0, 0, ×).

Correction with 1Hz signal:

Set addresses (A_3, A_2, A_1, A_0)=(1, 1, 1, 1).
Set Data (D_3, D_2, D_1, D_0)=(0, 1, 0, ×).

In each case, set addresses (A_3, A_2, A_1, A_0)=(1, 1, 0, 1), and set data (D_3, D_2, D_1, D_0)=(×, 0, ×, ×) to disable $\overline{\text{ALARM}}$ output before setting 16Hz or 1Hz signal.



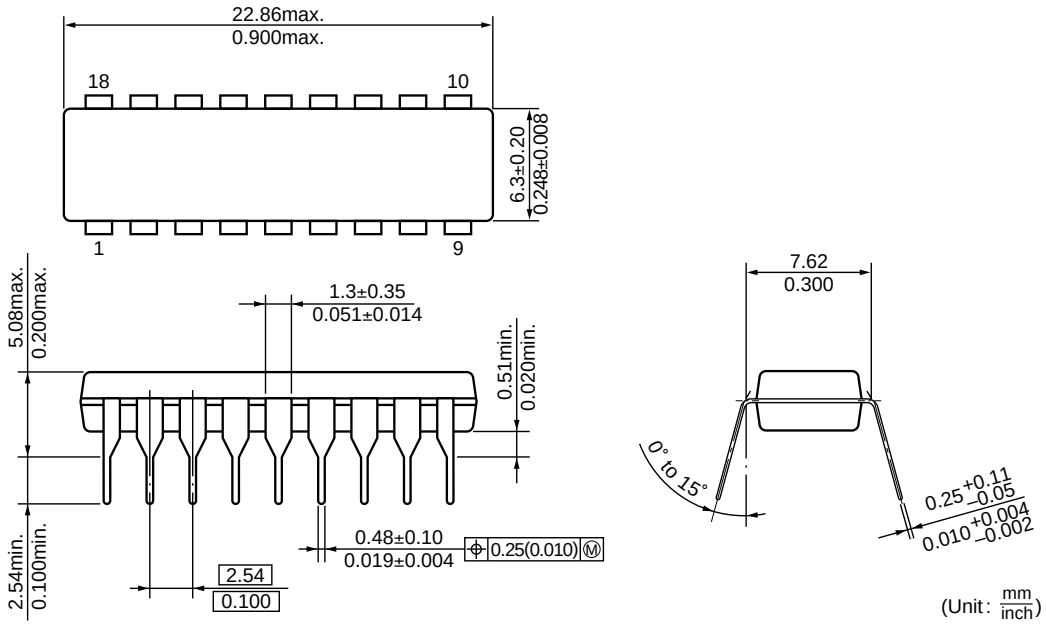
*) Values of C_1, C_2 and R are not absolute conditions but are indicated for reference only. Regard those C_1, C_2 and R values shown above as our optimum values in our experiments which employed MX38T.

Difference between the RP5C01 and the RP/RF5C01A

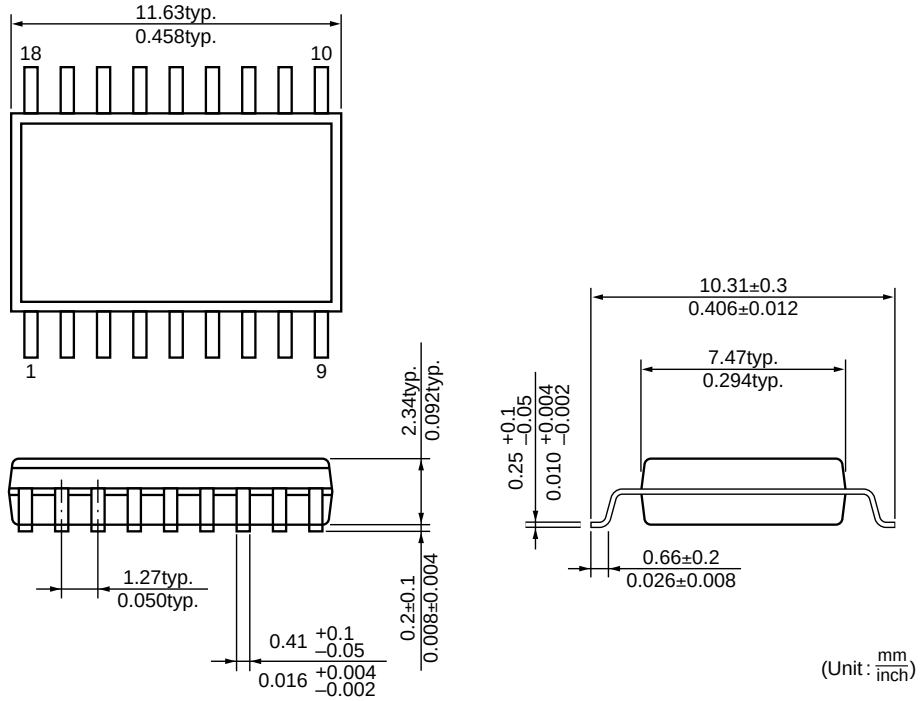
Since the RP5C01 and the RP/RF5C01A have different oscillator circuit characteristics, approximately 12 to 19ppm (31 to 41 seconds/month) of difference will result if the RP/RF5C01A are used with an external value that has been set to the RP5C01 oscillating characteristics. Therefore, determine a new external value for the RP/RF5C01A.

PACKAGE DIMENSIONS

• RP5C01A (18pin DIP)



• RP5C01A (18pin SOP)



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